

CLAIMS

What is claimed is:

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1. A method comprising the steps of:
 - a) identifying at least one statement within a synthesizable source code; and
 - b) synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement.
 2. The method of claim 1 wherein step b) includes the step of:
 - i) generating instrumentation logic to provide the instrumentation signal as if the source code included a corresponding signal assignment statement within a same executable branch of the source code as the identified statement.
 3. The method of claim 1 wherein step b) includes the steps of:
 - i) initializing a marker to a first value at the beginning of a process within the source code; and
 - ii) setting the marker to a second value within a same executable branch of the source code as the identified statement.
 4. The method of claim 3 further comprising the step of:
 - iii) assigning the value of the marker to the instrumentation signal at the end of the process.

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5. A method of generating a gate level design, comprising the steps of:
2 a) creating an instrumentation signal associated with at least one
3 synthesizable statement contained in a source code; and
4 b) synthesizing the source code into a gate-level design having the
5 instrumentation signal.

6. The method of claim 5 wherein step a) further comprises the step of:
2 i) inserting a unique variable assignment statement into the
3 source code, wherein the variable assignment statement is adjacent to at least
4 one associated sequential statement; and
5 ii) inserting a unique output signal assignment statement into the
6 source code, wherein the unique output signal is assigned a value associated
7 with the unique variable.

7. The method of claim 6 wherein the variable is assigned a first value in
2 step a)i), the method further comprising the step of:
3 iii) modifying the source code to initialize the unique variable to a
4 second value.

8. The method of claim 5 wherein step a) is repeated to create a unique
2 instrumented output signal for each list of sequential statements in the
3 source code, wherein each list corresponds to a synthesizable executable
4 branch of the source code.

1 9. The method of claim 5 further comprising the step of:
2 c) generating cross-reference instrumentation data mapping each
3 statement in a selected list to the instrumented output signal associated with
4 that list for every list in the source code.

1 10. The method of claim 9 further comprising the steps of:
2 d) simulating the gate level design using at least one of the
3 instrumentation signals to establish a simulation breakpoint.

1 11. The method of claim 5 further comprising the steps of:
2 c) displaying the source code, wherein at least one statement
3 within a selected list is highlighted if the instrumentation signal
4 corresponding to the selected list changes to a pre-determined value.

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12/ A method of generating a gate-level netlist, comprising the steps of:
2 a) receiving source code including synthesizable statements;
3 b) inserting a unique local variable assignment statement into the
4 source code for each branch of code having a list of at least one sequential
5 statement, wherein the unique local variable assignment statement is
6 adjacent to at least one statement within the list;
7 c) inserting a corresponding instrumentation signal assignment
8 statement into the source code for each of the inserted local variables,
9 wherein the instrumentation signal is assigned a value of the corresponding
10 unique local variable; and

11 d) synthesizing the source code into a gate-level design including
12 the instrumentation signals.

1 13. The method of claim 12 wherein step b) further comprises the steps of:

2 i) assigning each unique local variable a first value; and

3 ii) initializing each local variable with second value.

1 14. The method of claim 12 further comprising the step of

2 e) mapping every statement within a selected list to the

3 corresponding instrumentation signal for that selected list as cross-reference

4 instrumentation data.

1 15. The method of claim 12 further comprising the steps of:

2 e) setting a breakpoint at a selected statement of the source code;

3 f) identifying the instrumentation signal corresponding to the list

4 associated with the selected statement as a breakpoint signal; and

5 g) simulating the gate-level design, wherein simulation is halted at

6 a simulation cycle that results in the breakpoint signal transitioning to a

7 pre-determined value.

Sub. 16. A method of generating a gate level netlist, comprising the steps of:

2 a) receiving source code including synthesizable statements;

3 b) modifying the source code to generate a corresponding sampled

4 version of each signal event in a selected process;

5 c) modifying the source code to duplicate the selected process;

- 6 d) replacing each occurrence of a selected signal event with the
7 corresponding sampled version in the duplicated process;
8 e) replacing each list of sequential statements within an executable
9 branch of the duplicated process with a unique variable assignment
10 statement;
11 f) modifying the duplicated process to include an instrumentation
12 signal assignment for each unique variable; and
13 g) synthesizing the modified source code into a gate-level design.

- 1 17. The method of claim 16 wherein step e) further comprises the steps of:
2 i) assigning the unique variables a first value; and
3 ii) initializing the unique variables with second value.

- 1 18. The method of claim 16 further comprising the step of
2 e) mapping every statement within each selected list to its
3 corresponding instrumentation signal.

- 1 19. The method of claim 16 further comprising the steps of:
2 h) setting a breakpoint at a selected statement of the source code;
3 i) identifying the instrumentation signal corresponding to the list
4 associated with the selected statement as a breakpoint signal; and
5 j) simulating the gate-level design, wherein simulation is halted at
6 a simulation cycle that results in a transition of the breakpoint signal to a
7 pre-determined value.

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20. A method of debugging a gate-level design including the steps of:
- a) setting a breakpoint at a selected statement of a synthesizable source code;
 - b) inserting a local variable assignment statement adjacent to at least one statement in a list of sequential statements, wherein the list corresponds to an executable branch of the source code including the selected statement;
 - c) modifying the source code to include an instrumentation signal assignment statement for the local variable; and
 - d) generating a gate-level design from the modified source code.

21. The method of claim 20 further comprising the steps of:
- e) simulating the gate-level design, wherein simulation is halted at a simulation cycle that results in a transition of the instrumentation signal to a pre-determined value.

22. The method of claim 20 wherein step b) further comprises the steps of:

- i) assigning the local variable a first value; and
- ii) initializing the local variable with second value.

23. The method of claim 20 further comprising the step of

- e) mapping every statement within the executable branch of source code to the instrumentation signal.

1 24. A method of simulating a gate-level design comprising the steps of:

2 a) identifying a sensitivity list of a process;

3 b) generating logic to identify signal events for any signal in the
4 sensitivity list; and

5 c) identifying the process as active during simulation when a
6 signal event occurs for any signal in the sensitivity list.

1 25. The method of claim 24 wherein step c) further comprises the step of:

2 i) highlighting a source code description of the process displayed
3 during simulation.

1 26. The method of claim 24 wherein step b) further comprises the step of:

2 i) sampling each signal in the sensitivity list to generate
3 corresponding instrumented signals; and

4 ii) comparing each signal in the sensitivity list with its
5 corresponding instrumented signal to test each signal in the sensitivity list for
6 an event.

1 27. The method of claim 26 wherein step c) further comprises the step of:

2 i) generating an active process output signal defined by logically
3 ORing the results of the comparisons.

1 28. A storage medium having stored therein processor executable

2 instructions for generating a gate-level design from a register transfer level

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3 (RTL) synthesizable source code, wherein when executed the instructions
4 enable the processor to synthesize the source code into a gate-level netlist
5 including at least one instrumentation signal, wherein the instrumentation
6 signal is indicative of an execution status of at least one synthesizable
7 statement of the source code.

1 29. The storage medium of claim 28 wherein the processor performs the
2 steps of:

3 i) inserting a unique variable assignment statement into the
4 source code, wherein the variable assignment statement is adjacent to at least
5 one associated sequential statement; and

6 ii) inserting a unique output signal assignment statement into the
7 source code, wherein the unique output signal is assigned a value associated
8 with the unique variable.

1 ~~30.~~ A storage medium having stored therein processor executable
2 instructions for generating a gate-level design from a register transfer level
3 (RTL) synthesizable source code, wherein when executed the instructions
4 enable the processor to perform the steps of:

5 a) inserting a unique local variable assignment statement into the
6 source code for each branch of code having a list of at least one sequential
7 statement, wherein the unique local variable assignment statement is
8 adjacent to at least one statement within the list;

9 b) inserting a corresponding instrumentation signal assignment
10 statement into the source code for each of the inserted local variables,

09127534-073198

11 wherein the instrumentation signal is assigned a value of the corresponding
12 unique local variable; and
13 c) synthesizing the source code into a gate-level design including
14 the instrumentation signals.

1 31. The storage medium of claim 30 having stored therein further
2 instructions to enable the processor to perform the step of:
3 d) mapping every statement within each selected list to its
4 corresponding instrumentation signal.

1 ~~32.~~ A storage medium having stored therein processor executable
2 instructions for debugging a gate level design during simulation, wherein
3 when a breakpoint is set at a selected statement of a register transfer level
4 (RTL) synthesizable source code the instructions enable the processor to
5 perform the steps of:
6 a) inserting a local variable assignment statement adjacent to at
7 least one statement in a list of sequential statements within the source code,
8 wherein the list corresponds to an executable branch of the source code
9 including the selected statement;
10 b) modifying the source code to include an instrumentation output
11 signal assignment statement for the local variable; and
12 c) generating a gate-level design from the modified source code.

42

- 1 33. The storage medium of claim 32 having stored therein further
2 instructions to enable the processor to perform the step of:
3 d) mapping every statement within each selected list to its
4 corresponding instrumentation signal.

09127584-073198

43